REMARKS

Claims 1-18 remain in the application for consideration of the Examiner.

Reconsideration and withdrawal of the outstanding rejections are respectfully requested in light of the above amendments and following remarks.

Claims 1-18 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-18 of copending application 10/008,039.

Applicants respectfully request that this rejection be held in abeyance until at least one patent application has been patented. Furthermore, the rejection is premature since the claims may change during prosecution, and consequently, such a rejection may not be needed.

Turning now to the art rejections, Claims 1, 3-7, 9, and 11-18 were rejected under 35 U.S.C. §102(b) as being anticipated by Gabara; and Claims 1-2, 7, 8, and 10 were rejected under 35 U.S.C. §102(e) as being anticipated by Tinsley.

These rejections are respectively traversed.

It is respectfully submitted that Gabara does not disclose or suggest the presently claimed invention including the constant current source.

The Examiner alleges that Gabara discloses current source, MN3; however, this is not a constant current source.

With respect to Tinsley, Applicants note that this rejection was made under 35 U.S.C. §102(e). This section of the statue requires a disclosure of another.

In this connection, both the patent to Tinsley and the current patent have a common inventor, namely Steven Tinsley.

Consequently, the patent to Tinsley is not a patent to another. This rejection is improper.

It is respectfully submitted that Claims 1-18 patentably define over the applied references.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claims 1, 12, and 18 have been amended as follows:

1. A driver circuit for driving a load with a differential signal, comprising:

a first output drive portion operably coupled to a power supply rail;

a second output drive portion coupled to the first output drive portion, a low voltage differential input signal, and further comprising output terminals coupled to the load, and operably coupled with

a constant current source, wherein the second output drive portion is operable to switch alternate polarity terminals of the load to the current source; and

a common mode compensation circuit coupled to the output terminals of the second output drive portion and the first output drive portion, wherein the common mode compensation circuit is operable to detect a common mode voltage associated with the load and generate a compensation signal in response thereto, wherein the first output drive portion is operable to vary an impedance associated therewith in response to the compensation signal, thereby regulating a common mode voltage associated with the load, whereby the differential signal is transmitted to the load at a high rate of speed with a high compliance of the common mode output even at high current loading conditions, while maintaining a simple pre-drive circuit with a wide common mode range.

12. A driver circuit for driving a load with a differential signal, comprising:

a voltage mode output circuit operably coupled to a power supply rail;

a current mode switch circuit coupled to the voltage mode output circuit, a low voltage differential input signal, and further comprising output terminals coupled to the load, and operably coupled with a constant current source, wherein the current mode switch circuit is operable to switch alternate polarity terminals of the load to the constant current source; and

a common mode compensation circuit coupled to the output terminals of the current mode switch circuit and the voltage mode output circuit, wherein the common

mode compensation circuit is operable to detect a common mode voltage associated with the load and generate a compensation signal in response thereto, and wherein the voltage mode output circuit is operable to vary an impedance associated therewith in response to the compensation signal, thereby regulating a common mode voltage associated with the load, whereby the differential signal is transmitted to the load at a high rate of speed with a high compliance of the common mode output even at high current loading conditions, while maintaining a simple pre-drive circuit with a wide common mode range.

18. A method of driving a differential signal for high speed data transmission in transceiver, converter, and repeater devices comprising:

detecting a dc voltage associated with the differential signal across a load with a common mode voltage monitor circuit to provide a common mode voltage associated with a node of a voltage divider coupled across the terminals of the load;

applying the common mode voltage and a reference voltage to a common mode compensation circuit;

generating a compensation signal based on the common mode voltage and the reference voltage;

applying the compensation signal to a voltage mode output circuit;

adjusting the impedance of the voltage mode output circuit in response to the compensation signal, thereby regulating the common mode voltage associated with the load at a level set by the reference voltage;

inputting a low voltage differential input signal from a pre-drive circuit and the voltage regulated output from the voltage mode output circuit, into a second output drive portion;

switching the transistors of the current mode switch circuit in response to the low voltage differential input signal, between low and high conduction levels established by the voltage mode output circuit impedance and a constant current source, thereby conducting a current which flows from the voltage mode output circuit, thru the load, and the current mode switch circuit, and a current which flows thru the voltage mode output circuit and the current mode switch circuit; and

transmitting a differential signal to the load at a high rate of speed, with a high compliance of the common mode output even at high current loading conditions, while maintaining a simple pre-drive circuit design with a wide common mode range.